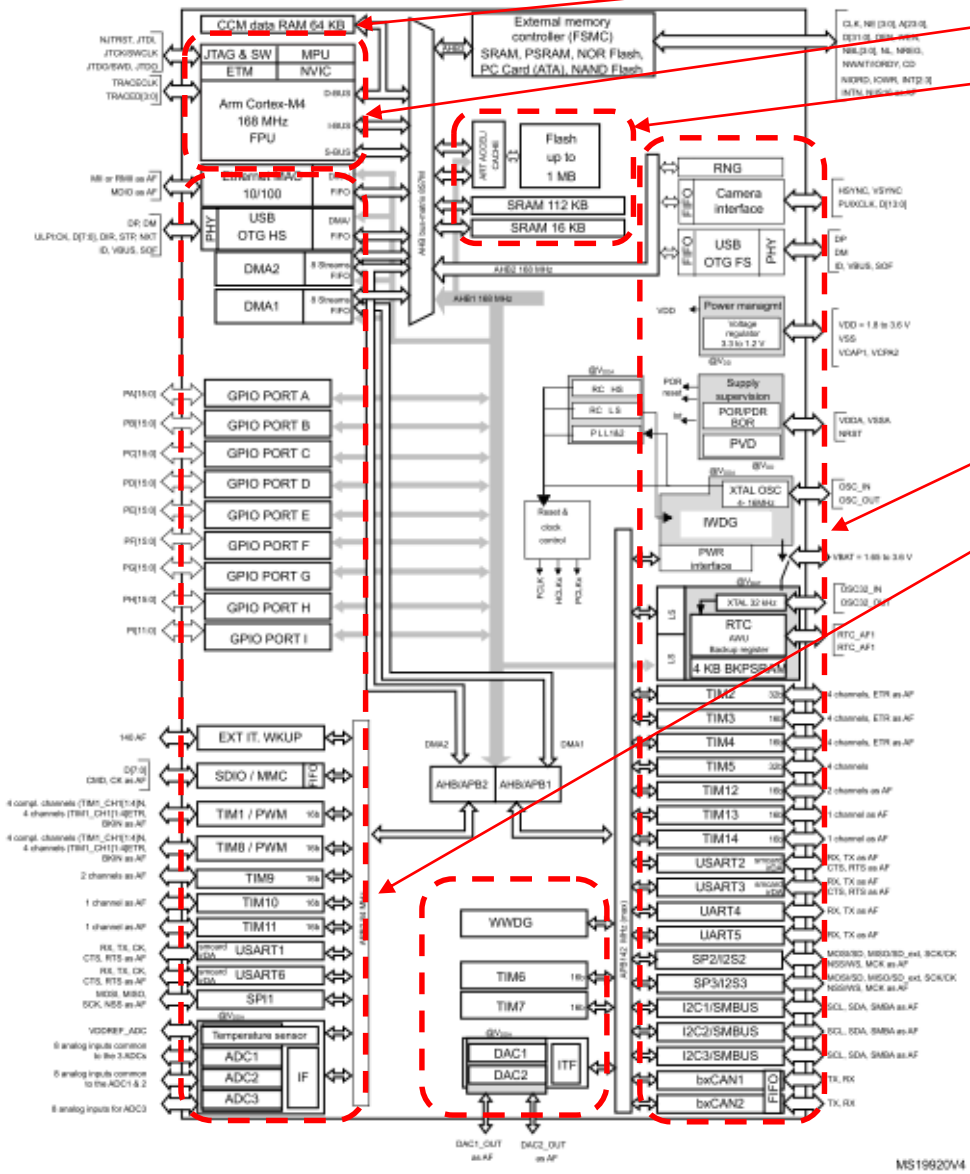
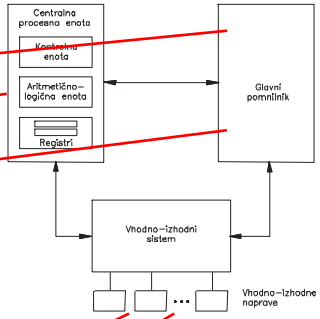
STM32F407 Discovery

Vhodno / izhodne naprave

USART Serijska komunikacija

STM32F407VG





Delo na STM32F4 razvojnem sistemu

Priključitev :

- **Mini USB** priklop na **krajši stranici**, svetita rdeči **LED** diodi

Poseben začetni projekt za *STM32F4* (e-učilnica) :

- ***dodajanje vsebine (template.s):***

'template.s - STM32CubeIDE

avigate Search Project Run Window Help

template.s

```
54
55 _start:
56     // Enable GPIOD Peripheral Clock (bit 3 in AHB1ENR register)
57     ldr r6, = RCC_AHB1ENR       // Load peripheral clock reg address to r6
58     ldr r5, [r6]                // Read its content to r5
59     orr r5, #0x00000008          // Set bit 3 to enable GPIOD clock
60     str r5, [r6]                // Store result in peripheral clock register
61
62     // Make GPIOD Pin12 as output pin (bits 25:24 in MODER register)
63     ldr r6, = GPIOD_MODER       // Load GPIOD MODER register address to r6
64     ldr r5, [r6]                // Read its content to r5
65     bic r5, #0x3000000          // Clear bits 24, 25 for P12
66     orr r5, #0x01000000         // Write 01 to bits 24, 25 for P12
67     str r5, [r6]                // Store result in GPIOD MODER register
68
69     // Set GPIOD Pin12 to 1 (bit 12 in ODR register)
70     ldr r6, = GPIOD_ODR         // Load GPIOD output data register
71     ldr r5, [r6]                // Read its content to r5
72     orr r5, #0x1000              // write 1 to pin 12
73     str r5, [r6]                // Store result in GPIOD output data register
74
75     // Set GPIOD Pin12 to 0 (bit 12 in ODR register)
76     ldr r6, = GPIOD_ODR         // Load GPIOD output data register
77     ldr r5, [r6]                // Read its content to r5
78     bic r5, #0x1000             // write 0 to pin 12
79     str r5, [r6]                // Store result in GPIOD output data register
80
81 loop:
82     nop                         // No operation. Do nothing.
83     b loop                      // Jump to loop
84
```

STM32 CubeIDE, STM32F4 (izbrana dokumentacij

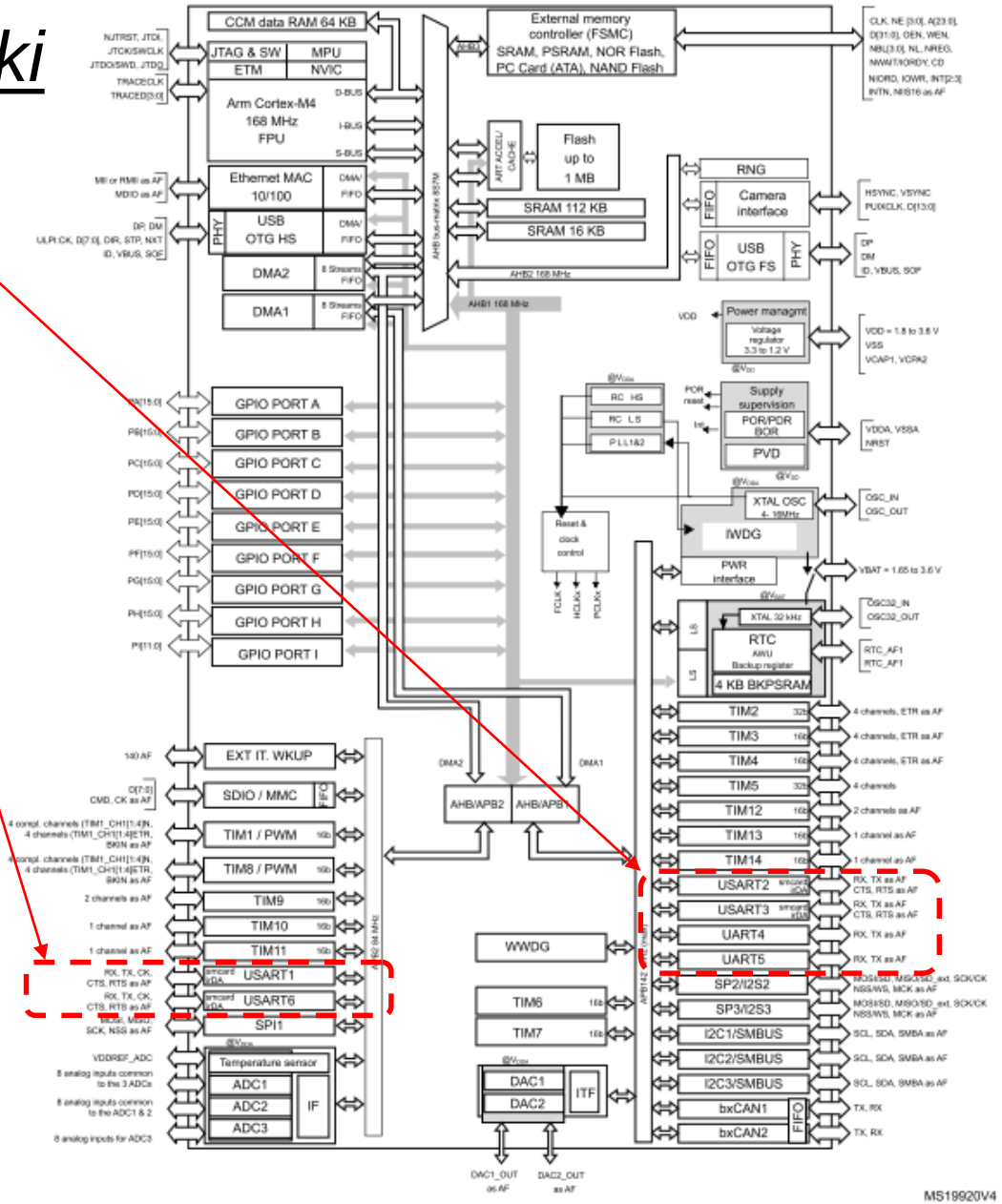
--------- Razvojni sistem ----------

- STM32 CubeIDE
- ORLab-STM32 - GitHub repozitorij
- User Manual Discovery kit stm32f407vg Uploaded 8/11/21, 12.58
- DataSheet_stm32f407vg Uploaded 8/11/21, 12.56
- Reference Manual rm0090-stm32f407417 Uploaded 8/11/21, 12.57
- Programming_Manual_pm0214-stm32-cortexm4-mcus-and-mpu
- Arm Cortex-M4 Processor Datasheet Short Uploaded 29/10/21, 15.00

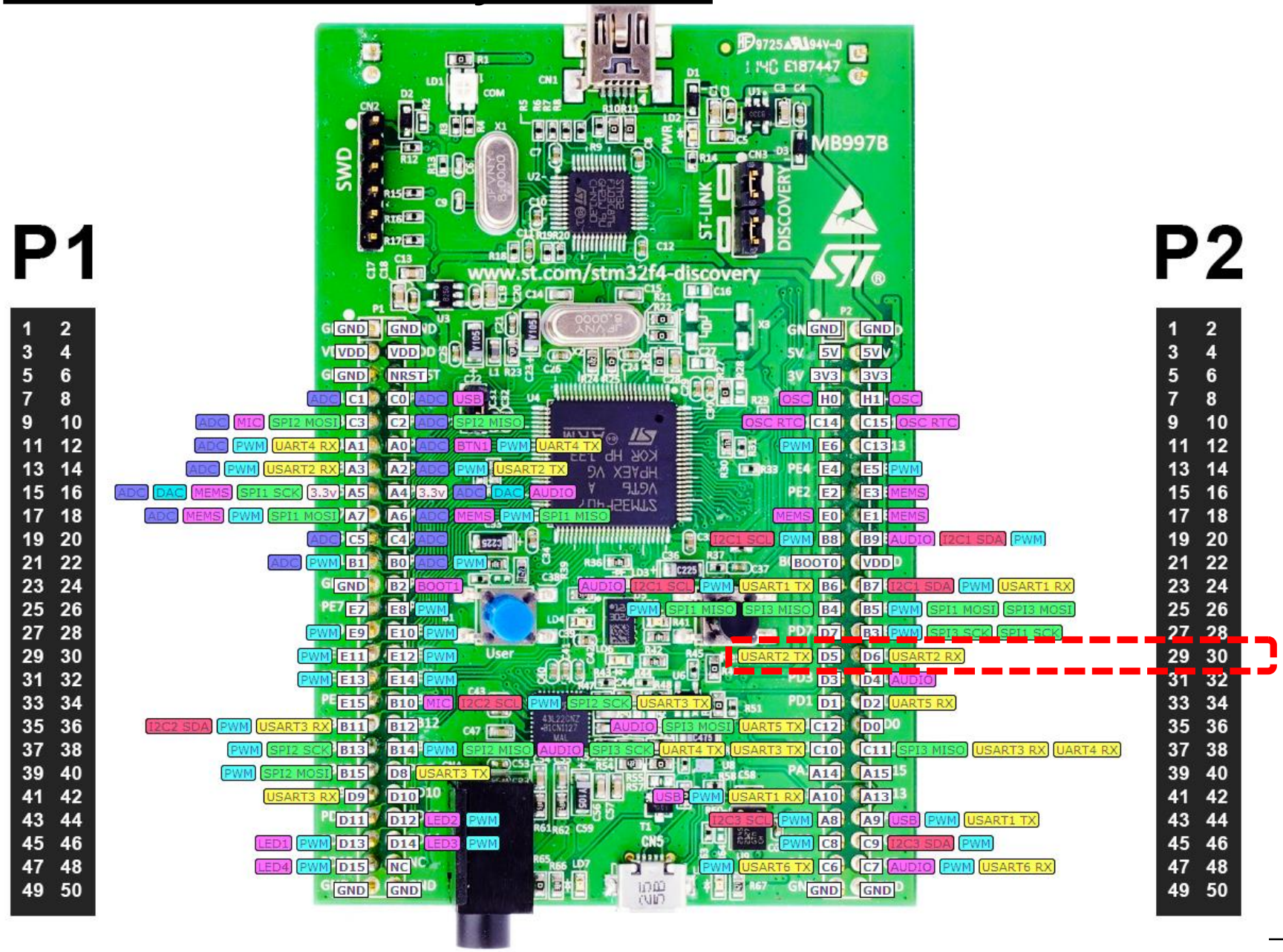
--------- Cortex-M arhitektura, zbirnik ----------

- ARM Cortex-M for Beginners ARM 2017 Uploaded 29/10/21, 14.50

Serijski vmesniki
USART



STM32F4 Discovery - Pinout



Vira: Reference manual & Datasheet

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RM0090
Reference manual

STM32F405/415, STM32F407/417, STM32F427/437 and STM32F429/439 advanced Arm®-based 32-bit MCUs

30 Universal synchronous asynchronous receiver transmitter (USART)

30.3.6 Multiprocessor communication

30.3.8 LIN (local interconnection network) mode

30.3.9 USART synchronous mode

30.3.10 Single-wire half-duplex communication

30.3.11 Smartcard

30.3.12 IrDA SIR ENDEC block

30.3.13 Continuous communication using DMA

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STM32F405xx STM32F407xx

Arm® Cortex®-M4 32b MCU+FPU, 210DMIPS, up to 1MB Flash/192+4KB RAM, USB OTG HS/FS, Ethernet, 17 TIMs, 3 ADCs, 15 comm. interfaces & camera

Datasheet - production data

Table 9. Alternate function mapping (continued)

Table 7. STM32F40xxx pin and ball definitions(1) (continued)

USART shema

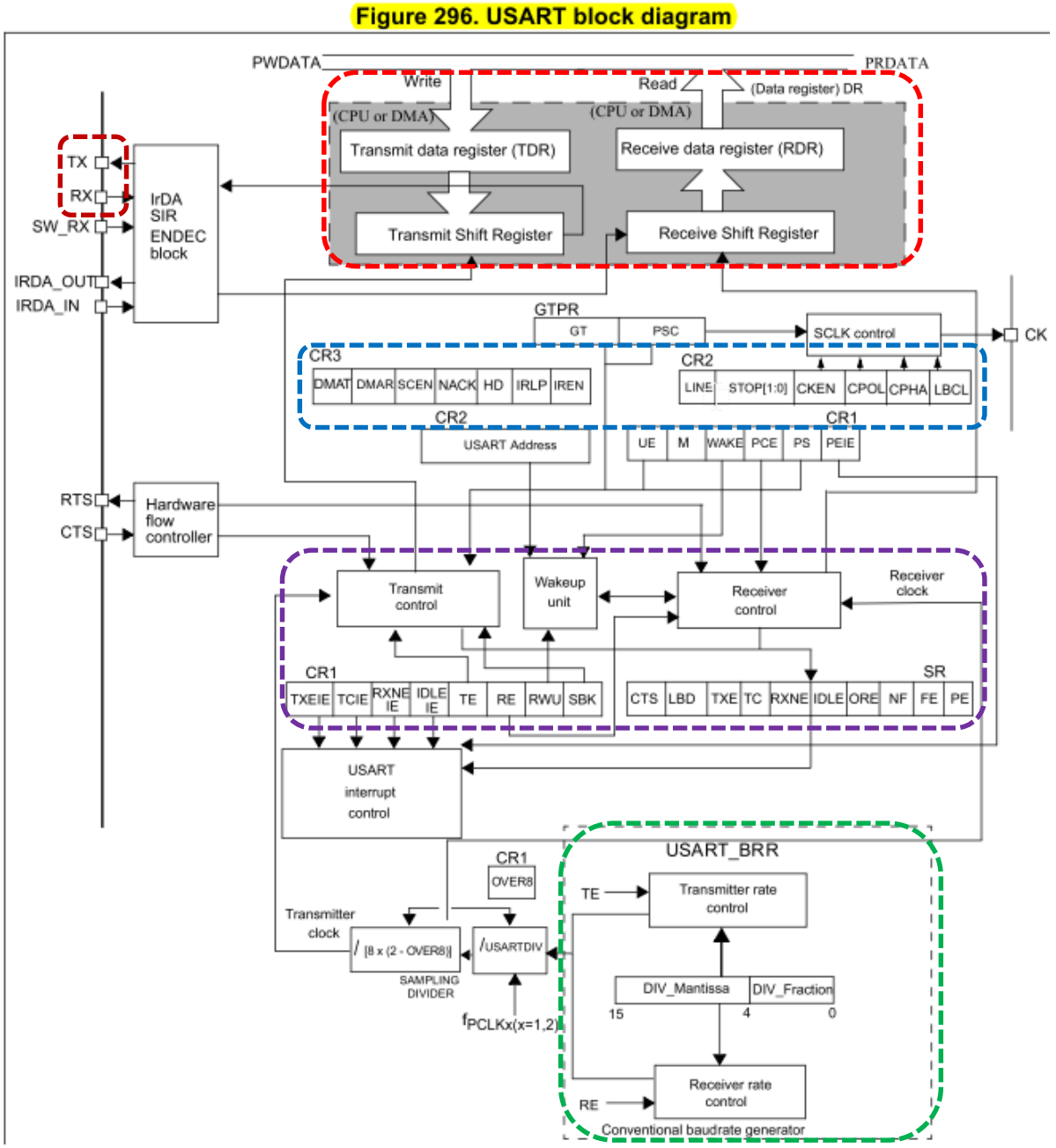
Figure 296. USART block diagram
PWDATA
PRDATA
Write
Read
(Data register) DR
(CPU or DMA)
(CPU or DMA)
Transmit data register (TDR)
Receive data register (RDR)
Transmit Shift Register
Receive Shift Register
TX
RX
SW_RX
IrDA SIR ENDEC block
IRDA_OUT
IRDA_IN
GTPR
GT
PSC
SCLK control
CK
CR3
CR2
DMAT DMAR SCEN NACK HD IRLP IREN
LINE STOP[1:0] CKEN CPOL CPHA LBCL
CR2
CR1
USART Address
UE M WAKE PCE PS PEIE
RTS
CTS
Hardware flow controller
Transmit control
Wakeup unit
Receiver control
Receiver clock
CR1
SR
TXEIE TCIE RXNE IE IDLE IE TE RE RWU SBK
CTS LBD TXE TC RXNE IDLE ORE NF FE PE
USART interrupt control
USART_BRR
CR1
OVER8
TE
Transmitter rate control
Transmitter clock
/ [8 x (2 - OVER8)]
/USARTDIV
SAMPLING DIVIDER
fPCLKx(x=1,2)
DIV_Mantissa
DIV_Fraction
15
4
0
RE
Receiver rate control
Conventional baudrate generator

USART (Registri za nastavitve GPIO AF)

Table 9. Alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10 /11	I2C1/2/3	SPI1/SPI2/ I2S2/I2S2e xt	SPI3/I2Sext /I2S3	USART1/2/3/ I2S3ext	UART4/5/ USART6	CAN1/2 TIM12/13/ 14	OTG_FS/ OTG_HS
Port D	PD0	-	-	-	-	-	-	-	-	-	CAN1_RX	-
	PD1	-	-	-	-	-	-	-	-	-	CAN1_TX	-
	PD2	-	-	TIM3_ETR	-	-	-	-	-	UART5_RX	-	-
	PD3	-	-	-	-	-	-	-	USART2_CTS	-	-	-
	PD4	-	-	-	-	-	-	-	USART2_RTS	-	-	-
	PD5	-	-	-	-	-	-	-	USART2_TX	-	-	-
	PD6	-	-	-	-	-	-	-	USART2_RX	-	-	-
	PD7	-	-	-	-	-	-	-	USART2_CK	-	-	-
	PD8	-	-	-	-	-	-	-	USART3_TX	-	-	-
	PD9	-	-	-	-	-	-	-	USART3_RX	-	-	-
	PD10	-	-	-	-	-	-	-	USART3_CK	-	-	-
	PD11	-	-	-	-	-	-	-	USART3_CTS	-	-	-
	PD12	-	-	TIM4_CH1	-	-	-	-	USART3_RTS	-	-	-
	PD13	-	-	TIM4_CH2	-	-	-	-	-	-	-	-
	PD14	-	-	TIM4_CH3	-	-	-	-	-	-	-	-
	PD15	-	-	TIM4_CH4	-	-	-	-	-	-	-	-

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STM32F405xx STM32F407xx

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Datasheet - production data

USART *(Registri za nastavitve GPIO AF)*

Table 7. STM32F40xxx pin and ball definitions(1) (continued)

Pin number						Pin name (function after reset)(2)	Pin type	I / O structure	Notes	Alternate functions
LQFP64	WLCSP90	LQFP100	LQFP144	UFBGA176	LQFP176					
-	A4	85	118	D10	146	PD4	I/O	FT	-	FSMC_NOE/ USART2_RTS/ EVENTOUT
-	C6	86	119	C11	147	PD5	I/O	FT	-	FSMC_NWE/USART2_TX/ EVENTOUT
-	-	-	120	D8	148	V_{SS}	S	-	-	-
-	-	-	121	C8	149	V_{DD}	S	-	-	-
-	B5	87	122	B11	150	PD6	I/O	FT	-	FSMC_NWAIT/ USART2_RX/ EVENTOUT

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STM32F405xx STM32F407xx

Arm® Cortex®-M4 32b MCU+FPU, 210DMIPS, up to 1MB Flash/192+4KB RAM, USB OTG HS/FS, Ethernet, 17 TIMs, 3 ADCs, 15 comm. interfaces & camera

Datasheet - production data

USART *(Registri za nastavitve GPIO AF)*

8.4 GPIO registers

This section gives a detailed description of the GPIO registers.
For a summary of register bits, register address offsets and reset values, refer to *Table 39*.

The GPIO registers can be accessed by byte (8 bits), half-words (16 bits) or words (32 bits).

8.4.1 GPIO port mode register (GPIOx_MODER) (x = A..I/J/K)

Address offset: 0x00

Reset values:

- 0xA800 0000 for port A
- 0x0000 0280 for port B
- 0x0000 0000 for other ports

PD6, PD5

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MODER15[1:0]		MODER14[1:0]		MODER13[1:0]		MODER12[1:0]		MODER11[1:0]		MODER10[1:0]		MODER9[1:0]		MODER8[1:0]	
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MODER7[1:0]		MODER6[1:0]		MODER5[1:0]		MODER4[1:0]		MODER3[1:0]		MODER2[1:0]		MODER1[1:0]		MODER0[1:0]	
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bits 2y:2y+1 **MODERy[1:0]:** Port x configuration bits (y = 0..15)

These bits are written by software to configure the I/O direction mode.

00: Input (reset state)
01: General purpose output mode
10: Alternate function mode
11: Analog mode

USART *(Registri za nastavitve GPIO AF)*

8.4.9 GPIO alternate function low register (GPIOx_AFRL) (x = A..I/J/K)

Address offset: 0x20

Reset value: 0x0000 0000

PD6, PD5

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AFRL7[3:0]				AFRL6[3:0]				AFRL5[3:0]				AFRL4[3:0]			
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AFRL3[3:0]				AFRL2[3:0]				AFRL1[3:0]				AFRL0[3:0]			
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bits 31:0 **AFRLy:** Alternate function selection for port x bit y (y = 0..7)

These bits are written by software to configure alternate function I/Os

AFRLy selection:

0000: AF0	1000: AF8
0001: AF1	1001: AF9
0010: AF2	1010: AF10
0011: AF3	1011: AF11
0100: AF4	1100: AF12
0101: AF5	1101: AF13
0110: AF6	1110: AF14
0111: AF7	1111: AF15

USART – stanje , nastavitve

Table 149. USART register map and reset values

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	USART_SR	Reserved																						CTS	LBD	TXE	TC	RXNE	IDLE	ORE	NF	FE	PE
	Reset value																							0	0	1	1	0	0	0	0	0	0
0x04	USART_DR	Reserved																						DR[8:0]									
	Reset value																							0	0	0	0	0	0	0	0	0	0
0x08	USART_BRR	Reserved																		DIV_Mantissa[15:4]										DIV_Fraction [3:0]			
	Reset value																			0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0C	USART_CR1	Reserved																		OVER8	Reserved	UE	M	WAKE	PCE	PS	PEIE	TXEIE	TCIE	RXNEIE	IDLEIE	TE	RE	RWU	SBK
	Reset value																			0		0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x10	USART_CR2	Reserved																		LINEN	STOP [1:0]		CLKEN	CPOL	CPHA	LBCL	Reserved	LBDIE	LBDL	Reserved	ADD[3:0]			
	Reset value																			0	0	0	0	0	0	0		0	0		0	0	0	0

Osnovni registri za delovanje USART naprave:

- **USART_SR**
  - **TXE=1, pošlji znak | RXNE=1 prejet znak**
- **USART_DR : Data Register**
  - **READ: Received Char | WRITE: Send Char**
- **USART_BRR : BaudRate Register**
  - **DIV_Mantissa,DIV_Fraction = delilnik frekvence**
- **USART_CR1 : Control Register 1**
  - **ENABLE USART, TX, RX bits**

USART (Registri za nastavitve delovanja)

30.6 USART registers

Refer to *Section 1.1: List of abbreviations for registers* for registers for a list of abbreviations used in register descriptions.

The peripheral registers have to be accessed by half-words (16 bits) or words (32 bits).

30.6.1 Status register (USART_SR)

Address offset: 0x00

Reset value: 0x0000 00C0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						CTS	LBD	TXE	TC	RXNE	IDLE	ORE	NF	FE	PE
						rc_w0	rc_w0	r	rc_w0	rc_w0	r	r	r	r	r

Bit 7 **TXE**: Transmit data register empty

This bit is set by hardware when the content of the TDR register has been transferred into the shift register. An interrupt is generated if the TXEIE bit =1 in the USART_CR1 register. It is cleared by a write to the USART_DR register.

0: Data is not transferred to the shift register

1: Data is transferred to the shift register)

Note: This bit is used during single buffer transmission.

Bit 5 **RXNE**: Read data register not empty

This bit is set by hardware when the content of the RDR shift register has been transferred to the USART_DR register. An interrupt is generated if RXNEIE=1 in the USART_CR1 register. It is cleared by a read to the USART_DR register. The RXNE flag can also be cleared by writing a zero to it. This clearing sequence is recommended only for multibuffer communication.

0: Data is not received

1: Received data is ready to be read.

USART *(Registri za nastavitve delovanja)*

30.6.2 Data register (USART_DR)

Address offset: 0x04

Reset value: 0xXXXX XXXX

Bits 31:9 Reserved, must be kept at reset value

Bits 8:0 **DR[8:0]**: Data value

Contains the Received or Transmitted data character, depending on whether it is read from or written to.

USART (Registri za nastavitve delovanja)

30.6.3 Baud rate register (USART_BRR)

Note: The baud counters stop counting if the TE or RE bits are disabled respectively.

Address offset: 0x08

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIV_Mantissa[11:0]												DIV_Fraction[3:0]			
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bits 31:16 Reserved, must be kept at reset value

Bits 15:4 **DIV_Mantissa[11:0]**: mantissa of USARTDIV

These 12 bits define the mantissa of the USART Divider (USARTDIV)

$52{,}0625 = 110100{,}0001_2$

Bits 3:0 **DIV_Fraction[3:0]**: fraction of USARTDIV

These 4 bits define the fraction of the USART Divider (USARTDIV). When OVER8=1, the DIV_Fraction3 bit is not considered and must be kept cleared.

Table 136. Error calculation for programmed baud rates at f_{PCLK} = 16 MHz or f_{PCLK} = 24 MHz, oversampling by 16(1)

Oversampling by 16 (OVER8 = 0)							
Baud rate		f_{PCLK} = 16 MHz			f_{PCLK} = 24 MHz		
S.No	Desired	Actual	Value programmed in the baud rate register	% Error = (Calculated - Desired) B.rate / Desired B.rate	Actual	Value programmed in the baud rate register	% Error
1	1.2 KBps	1.2 KBps	833.3125	0	1.2	1250	0
2	2.4 KBps	2.4 KBps	416.6875	0	2.4	625	0
3	9.6 KBps	9.598 KBps	104.1875	0.02	9.6	156.25	0
4	19.2 KBps	19.208 KBps	52.0625	0.04	19.2	78.125	0
5	38.4 KBps	38.369 KBps	26.0625	0.08	38.4	39.0625	0
6	57.6 KBps	57.554 KBps	17.375	0.08	57.554	26.0625	0.08

USART *(Registri za nastavitve delovanja)*

30.6.4 Control register 1 (USART_CR1)

Address offset: 0x0C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OVER8	Reserved	UE	M	WAKE	PCE	PS	PEIE	TXEIE	TCIE	RXNEIE	IDLEIE	TE	RE	RWU	SBK
rw	Res.	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit 13 **UE**: USART enable

When this bit is cleared, the USART prescalers and outputs are stopped and the end of the current byte transfer in order to reduce power consumption. This bit is set and cleared by software.

0: USART prescaler and outputs disabled

1: USART enabled

Bit 12 **M**: Word length

This bit determines the word length. It is set or cleared by software.

0: 1 Start bit, 8 Data bits, n Stop bit

1: 1 Start bit, 9 Data bits, n Stop bit

Note: The M bit must not be modified during a data transfer (both transmission and reception)

Bit 10 **PCE**: Parity control enable

This bit selects the hardware parity control (generation and detection). When the parity control is enabled, the computed parity is inserted at the MSB position (9th bit if M=1; 8th bit if M=0) and parity is checked on the received data. This bit is set and cleared by software. Once it is set, PCE is active after the current byte (in reception and in transmission).

0: Parity control disabled

1: Parity control enabled

Bit 3 **TE**: Transmitter enable

This bit enables the transmitter. It is set and cleared by software.

0: Transmitter is disabled

1: Transmitter is enabled

Note: During transmission, a "0" pulse on the TE bit ("0" followed by "1") sends a preamble (idle line) after the current word, except in smartcard mode.

When TE is set, there is a 1 bit-time delay before the transmission starts.

Bit 2 **RE**: Receiver enable

This bit enables the receiver. It is set and cleared by software.

0: Receiver is disabled

1: Receiver is enabled and begins searching for a start bit

USART (Registri za nastavitve delovanja)

30.6.5 Control register 2 (USART_CR2)

Address offset: 0x10

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res.	LINEN	STOP[1:0]		CLKEN	CPOL	CPHA	LBCL	Res.	LBDIE	LBDL	Res.	ADD[3:0]			
	rw	rw	rw	rw	rw	rw	rw		rw	rw	rw	rw	rw	rw	rw

Bits 13:12 **STOP**: STOP bits

These bits are used for programming the stop bits.

00: 1 Stop bit

01: 0.5 Stop bit

10: 2 Stop bits

11: 1.5 Stop bit

Note: The 0.5 Stop bit and 1.5 Stop bit are not available for UART4 & UART5.

USART – krmiljenje

Potrebni koraki za krmiljenje USART naprave:

1. **Vklop USART naprave**
   - **RCC_APB1ENR : b_{17}=1 (USART2 Enable Clock)**
2. **Nastavitev GPIO priključkov na AF (Alt. Function)**
   - **GPIOD_AFRL (AF Register): 0x07700000 (PD5,PD6)**
   - **GPIO_MODER (Mode Register): 0b10 on AF pins (PD5,PD6)**
3. **Nastavitev hitrosti delovanja (BaudRate)**
   - **USART2_BRR (BaudRate Register): $52{,}0625=110100{,}0001_2$**
4. **Sprožitev delovanja**
   - **USART2_CR1 (Control Register 1): TX, RX Enable bits**

5. Delovanje

Oddaja znaka:

- **USART2_SR: ko TXE=1, vpis znaka v USART2_DR**

Sprejem znaka:

- **USART2_SR: ko RXNE=1, preberi znak iz USART2_DR**

USART – krmiljenje

Naslovi registrov:

```
// RCC   base address is 0x40023800
.equ     RCC_BASE,   0x40023800
.equ     RCC_AHB1ENR,   0x30 // RCC AHB1 peripheral clock reg (page 180)
.equ     RCC_APB1ENR,   0x40 // RCC APB1 peripheral clock reg (page 183)

// GPIOD base address is 0x40020C00
.equ     GPIOD_BASE,   0x40020C00  // GPIOD base address)
.equ     GPIOD_MODER,   0x00       // GPIOD port mode register (page 281)
.equ     GPIOD_ODR,     0x14       // GPIOD output data register (page 283)
.equ     GPIOD_BSSR,     0x18      // GPIOD port set/reset register (page 284)
.equ     GPIOD_AFRL,     0x20      // GPIOD output data register (page 285)
.equ     GPIOD_AFRL_VALUE,     0x07700000    // AF7 on PD5,6

// USART2 base address is 0x40004400
.equ     USART2_BASE,   0x40004400 // USART2 base address)
.equ     USART2_SR,    0x00 // SR register (page 1007)
.equ     USART2_DR,    0x04 // SR register (page 1007)
.equ     USART2_BRR,   0x08 // BRR register (page 1010)
.equ     USART2_BRR_VAL,   (52<<4)+0b1010 // BRR register
.equ     USART2_CR1,   0x0C // CR1 register
.equ     USART2_CR1_VAL,   0x200C // CR1 register
```

CubeIDE – Registers okno

Name	Value
General Registers	
r0	0x0
r1	0x0
r2	0x0
r3	0x0
r4	0x0
r5	0x1000
r6	0x40020c14
r7	0x0
r8	0x0
r9	0x0
r10	0x0
r11	0x0
r12	0x0
sp	0x20020000
lr	0xffffffff
pc	0x800002a
xpsr	0x41000000

CubeIDE – SFR okno